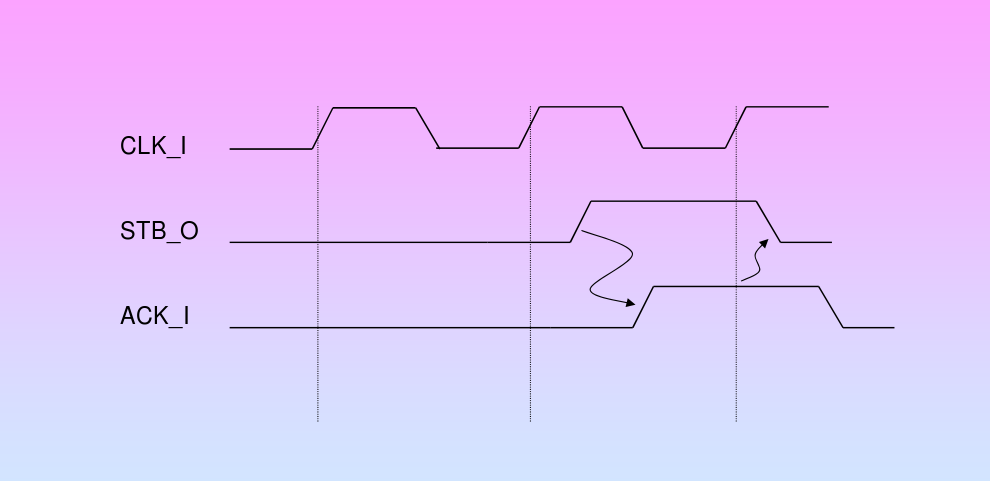


Wishbone architecture ( we got 4 masters and 5 slaves ) the slave is undecided yet ( prob depends on prorts):

Theory :

master initiates the communication by providing address and control signals to slave and then slave respond to master with specified address range.The INTERCON system provides interface between master and slave for data transfer between them.The SYSCON provides wishbone clock and reset signals for proper functioning of system.Fig1 shown above clearly describes the process.Wishbone INTERCON are designed to operate over infinite frequency range and can be described using hardware languages like VERILOG or VHDL

Hand Shaking protocol : 

the MASTER asserts [STB\_O] when it is ready to transfer data. [STB\_O]

remains asserted until the SLAVE asserts one of the cycle terminating signals [ACK\_I], [ERR\_I]

or [RTY\_I]. At every rising edge of [CLK\_I] the terminating signal is sampled. If it is asserted,

then [STB\_O] is negated. This gives both MASTER and SLAVE interfaces the possibility to

control the rate at which data is transferred.